What Is Claimed Is:

1. An array substrate device, comprising:

a gate line formed on a substrate extending along a first direction having a gate electrode;

a data line formed on the substrate extending along a second direction having a data pad disposed apart from a first end of the data line, the data and gate lines defining a pixel region;

a gate pad formed on the substrate disposed apart from a first end of the gate line;

a thin film transistor formed at a crossing region of the gate and data lines and including the gate electrode, a semiconductor layer, a source electrode, and a drain electrode;

a black matrix overlapping the thin film transistor, the gate line, and the data line except for a first portion of the drain electrode;

a first pixel electrode at the pixel region contacting the first portion of the drain electrode and the substrate;

a color filter on the first pixel electrode at the pixel region; and

a second pixel electrode on the color filter contacting the first pixel electrode.

2. The device according to claim 1, further comprising:

a first insulating layer covering the gate line and the gate electrode;

a second insulating layer covering the thin film transistor, the gate pad, the data line, and the data pad;

a third insulating layer covering the black matrix, wherein the second and third insulating layers expose the first portion of the drain electrode and have a plurality of first contact holes and a second contact hole to expose the gate and data pads, respectively, and the first, second, and third insulating layers have an opening and a third contact hole to expose the substrate in the pixel region and the first end of the gate line, respectively;

a double-layered gate pad terminal on the third insulating layer directly above the gate pad, the double-layered gate pad terminal includes two transparent conductive layers and contacts the gate pad through one of the first contact holes;

a double-layered data pad terminal on the third insulating layer directly above the data pad, wherein the double-layered data pad terminal includes two transparent conductive layers and contacts the data pad through the second contact hole; and

a double-layered connecting line, wherein the double-layered connecting electrode includes first and second connecting electrodes of transparent conductive material, and wherein the double-layered connecting electrode

contacts the gate pad and the first end of the gate line, respectively, through one of the first contact holes and through the third contact hole, thereby electrically connecting the gate pad to the gate line.

3. The device according to claim 2, further comprising a color filter pattern between the first and second connecting electrodes, wherein:

the color filter pattern includes a same material as the color filter and corresponds to the third contact hole;

the color filter pattern corresponds to one of the first contact holes through which the double-layered connecting electrode contacts the gate pad and which is disposed adjacent to the first end of the gate line; and

wherein the color filter pattern is formed of a color resin that has one of red, blue, and green colors.

4. The device according to claim 2, further comprising a storage metal layer on the first insulating layer over the gate line, wherein:

the second and third insulating layers expose a portion of the storage metal layer;

the first pixel electrode contacts the portion of the storage metal layer exposed by the second and third insulating layers; and

the storage metal layer and a portion of the gate line constitute a storage capacitor with the first insulating layer interposed between the storage metal layer and the gate line.

5. The device according to claim 4, further comprising a semiconductor pattern between the storage metal layer and the first insulating layer, wherein the semiconductor pattern includes an intrinsic amorphous silicon pattern and a doped amorphous silicon pattern.

6. The device according to claim 2, further comprising a plurality of semiconductor patterns between the gate pad and the first insulating layer, between the data line and the first insulating layer, and between the data pad and the first insulating layer, wherein each of the semiconductor patterns includes an intrinsic amorphous silicon pattern and a doped amorphous silicon pattern.

7. The device according to claim 1, wherein the first pixel electrode directly contacts the substrate.

8. The device according to claim 1, wherein the semiconductor layer includes an active layer of intrinsic amorphous silicon over the gate electrode and an ohmic contact layer of doped amorphous silicon on the active layer.

9. A method of forming an array substrate, comprising:

forming a gate line on a substrate extending along a first direction having a gate electrode extending from the gate line;

sequentially forming an active layer of intrinsic amorphous silicon and an ohmic contact layer of extrinsic amorphous silicon layer over the gate electrode;

simultaneously forming a data line, a data pad, a gate pad, a source electrode, and a drain electrode, the data line disposed to perpendicularly cross the gate line and defining a pixel region, wherein the gate electrode, the active and ohmic contact layers, and the source and drain electrode constitute a thin film transistor;

forming a black matrix to overlap the thin film transistor, the gate line, and the data line except for a first portion of the drain electrode;

forming a first transparent electrode layer to overlap the black matrix, the first transparent electrode contacting the portion of the drain electrode;

forming a color filter on the first transparent electrode layer in the pixel region and a color filter pattern above a first end of the gate line; and

forming a second transparent electrode layer along an entire surface of the substrate to cover the color filter, the color filter pattern, and the first transparent electrode layer.

10. The method according to claim 9, further comprising:

forming a first insulating layer on the substrate to cover the gate line and the gate electrode;

forming a second insulating layer along an entire surface of the substrate to cover the thin film transistor, the gate pad, the data pad, and the data line;

forming a third insulating layer along an entire surface of the substrate to cover the black matrix and the second insulating layer;

patterning the first, second, and third insulating layers to expose the substrate in the pixel region and to form plural first contact holes, a second contact hole, and a third contact hole, the first contact holes exposing the gate pad, the second contact hole exposing the data pad, and the third contact holes exposing the first end of the gate line, wherein patterning the second and third insulating layers expose the first portion of the drain electrode; and

patterning the first and second transparent electrode layers to form first and second pixel electrodes, double-layered gate, data pad terminals, and a double-layered connecting line;

wherein the double-layered gate pad terminal is disposed on the third insulation layer directly above the gate pad and includes two transparent conductive layers, and contacts the gate pad through one of the first contact holes;

wherein the double-layered data pad terminal is disposed on the third insulating layer directly above the data pad and includes two transparent conductive layers, and contacts the data pad through the second contact hole; and

wherein the double-layered connecting electrode includes first and second connecting electrodes of a transparent conductive material, and contacts the gate pad and the first end of the gate line, respectively, through one of the first contact holes and through the third contact hole, thereby electrically connecting the gate pad to the gate line.

11. The method according to claim 10, wherein:

forming the gate line and gate electrode uses a first mask;

forming the active and ohmic contact layers uses a second mask;

forming the data line, the data pad, the gate pad, and the source and drain electrodes uses a third mask;

forming the black matrix uses a fourth mask;

patterning the first, second, and third insulating layers uses a fifth mask; and

patterning the first and second transparent electrode layers uses a sixth mask.

12. The method according to claim 11, wherein forming the data and gate pads includes forming a storage metal layer above the gate line, and the storage metal layer and a portion of the gate line constitute a storage capacitor with the first insulating layer interposed between the storage metal layer and the gate line.

13. The method according to claim 12, wherein patterning the second and third insulating layers exposes a portion of the storage metal layer, and the first pixel electrode contacts the portion of the storage metal layer exposed by the second and third insulating layers.

14. The method according to claim 10, wherein:

the color filter pattern is disposed between the first and second connecting electrodes and corresponds to the third contact hole;

the color filter pattern corresponds to one of the first contact holes through which the double-layered connecting electrode contacts the gate pad and which is disposed adjacent to the first end of the gate line; and

the color filter and the color filter pattern are formed of a color resin that has one of red, blue, and green colors.

15. The method according to claim 9, wherein:

the thin film transistor is disposed at a crossing of the gate and data lines;

the data pad is disposed at one end of the data line;

the gate pad is disposed on the first insulating layer and spaced apart from one end of the gate line;

the source electrode extends from the data line onto one portion of the ohmic contact layer; and

the drain electrode is spaced apart from the source electrode onto the other portion of the ohmic contact layer.

16. The method according to claim 9, wherein:

the first pixel electrode directly contacts the substrate;

the first and second pixel electrodes constitute a sandwich pixel electrode with the interposed color filter; and

the data line, the data pad, the gate pad, the source electrode, and the drain electrode are formed of a metallic material selected from a group

consisting of chromium (Cr), molybdenum (Mo), copper (Cu), tungsten (W), titanium (Ti), and an alloy of any combination thereof.

17. A method of forming an array substrate, comprising:

forming a gate line extending along a first direction includes a gate electrode extending from the gate line using a first metal layer;

forming a first insulating layer on the substrate to cover the gate line and the gate electrode;

forming an intrinsic amorphous silicon layer, an extrinsic amorphous silicon layer, and a second metal layer on the first insulating layer;

patterning the intrinsic amorphous silicon layer, the extrinsic amorphous silicon layer, and the second metal layer to form a data line, a data pad, a gate pad, a source electrode, a drain electrode, and a plurality of semiconductor patterns, wherein the data line is disposed to perpendicularly cross the gate line and define a pixel region;

etching a portion of the extrinsic amorphous silicon pattern between the source and drain electrodes to from an active layer of intrinsic amorphous silicon pattern and an ohmic contact layer of extrinsic amorphous silicon pattern, wherein the gate electrode, the active and ohmic contact layers, and the source and drain electrodes constitute a thin film transistor at the crossings of the gate and data lines;

forming a black matrix to overlap the thin film transistor, the gate line, and the data line except for a first portion of the drain electrode;

forming a first transparent electrode layer to overlap the black matrix and contact the first portion of the drain electrode;

forming a color filter on the first transparent electrode layer in the pixel region and a color filter pattern above a first end of the gate line; and

forming a second transparent electrode layer to cover the color filter, the color filter pattern, and the first transparent electrode layer.

18. The method according to claim 17, wherein patterning the intrinsic and extrinsic amorphous silicon layers and the second metal layer includes forming a photoresist on the second metal layer and disposing a mask over the photoresist, and the mask includes a light-transmitting portion, a light-shielding portion, and a half-light-transmitting portion.

19. The method according to claim 17, further comprising:

forming a second insulating layer along an entire surface of the substrate to cover the thin film transistor, the gate pad, and the data pad;

forming a third insulating layer along an entire surface of the substrate to cover the black matrix and the second insulating layer;

patterning the first, second, and third insulating layers to expose the substrate in the pixel region and to form a plurality of first contact holes, a second contact hole and a third contact hole, the first contact holes exposing the gate pad, the second contact hole exposing the data pad, and the third contact holes exposing the first end of the gate line, wherein patterning the second and third insulating layers expose the first portion of the drain electrode; and

patterning the first and second transparent electrode layers to form first and second pixel electrodes, double-layered gate and data pad terminals, and a double-layered connecting line;

wherein the double-layered gate pad terminal is disposed on the third insulation layer directly above the gate pad and includes two transparent conductive layers, and contacts the gate pad through one of the first contact holes;

wherein the double-layered data pad terminal is disposed on the third insulating layer directly above the data pad and includes two transparent conductive layers, and contacts the data pad through the second contact hole; and

wherein the double-layered connecting electrode includes first and second connecting electrodes of a transparent conductive material, and contacts the gate pad and the first end of the gate line, respectively, through one of the

first contact holes and through the third contact hole, thereby electrically connecting the gate pad to the gate line.

20. The method according to claim 19, wherein:

forming the gate line and electrode uses a first mask;

patterning the intrinsic and extrinsic amorphous silicon layers and the second metal layer uses a second mask;

forming the black matrix uses a third mask;

patterning the first, second, and third insulating layers uses a fourth mask; and

patterning the first and second transparent electrode layers uses a fifth mask.

21. The method according to claim 19, wherein forming the data and gate pads includes forming a storage metal layer above the gate line, and the storage metal layer and a portion of the gate line constitute a storage capacitor with the first insulating layer interposed between the storage metal layer and the gate line.

22. The method according to claim 21, wherein patterning the second and third insulating layers exposes a portion of the storage metal layer, and the first pixel electrode contacts the portion of the storage metal layer exposed by the second and third insulating layers.

23. The method according to claim 18, wherein:

the data pad is disposed at a first end of the data line;

the gate pad is spaced apart from the first end of the gate line;

the source electrode extends from the data line to the pixel region;

the drain electrode is spaced apart from the source electrode; and

the semiconductor patterns each include an intrinsic amorphous silicon pattern and an extrinsic amorphous silicon pattern disposed beneath the patterned second metal layer.

24. The method according to claim 19, wherein the semiconductor patterns are disposed between the gate pad and the first insulating layer, between the data line and the first insulating layer, and between the data pad and the first insulating layer.

25. The method according to claim 19, wherein:

the color filter pattern is disposed between the first and second connecting electrodes and corresponds to the third contact hole;

the color filter pattern corresponds to one of the first contact holes through which the double-layered connecting electrode contacts the gate pad and which is disposed next to the one end of the gate line; and

the color filter and the color filter pattern are formed of a color resin that has one of red, blue, and green colors.

26. The method according to claim 19, wherein:

the first pixel electrode directly contacts the substrate;

the first and second pixel electrodes constitute a sandwich pixel electrode with the interposed color filter; and

the second metal layer is formed of one of chromium (Cr), molybdenum (Mo), copper (Cu), tungsten (W), titanium (Ti), and an alloy of any combination thereof.

27. An array substrate device having a color filter on a thin film transistor (COT) structure for use in a liquid crystal display device, comprising:

a substrate having a display area, a non-display area, and a boundary area, the boundary area disposed between the display area and the non-display area;

a plurality of gate lines on the substrate within the display area;

a plurality of gate pads on the substrate within the non-display area;

a plurality of gate link lines on the substrate disposed in the non-display area and in the boundary area connecting the gate lines to the gate pads;

a plurality of data lines crossing the gate lines and defining a plurality of pixel regions;

a plurality of thin film transistors each near the crossings of the gate and data lines and including a gate electrode, an active layer, a source electrode, and a drain electrode;

a black matrix disposed above the thin film transistors, the gate lines, and the data lines;

a plurality of color filters disposed in the pixel regions;

a light-shielding pattern disposed in the non-display area and the boundary area corresponding to the gate link lines and spaces between the gate link lines; and

a plurality of pixel electrodes disposed in the pixel regions, each of the pixel electrodes contacting the drain electrode of the thin film transistor.

28. The device according to claim 27, further comprising an interlayer insulator between the black matrix and the thin film transistors and includes an inorganic material selected from a group consisting of silicon nitride and silicon oxide.

29. The device according to claim 27, wherein the light-shielding pattern completely covers the spaces between the gate link lines to prevent light leakage.

30. The device according to claim 27, further comprising:

a seal pattern above the light-shielding pattern; and

an inorganic insulator between the seal pattern and the light-shielding pattern,

wherein the inorganic insulator includes a material selected from a group consisting of silicon nitride and silicon oxide.

31. The device according to claim 30, wherein the seal pattern directly contacts the gate link lines.

32. The device according to claim 27, wherein the pixel electrode includes a double-layered transparent conductive material including first and second layers, and each of the color filters is disposed between the first and second layers.

33. An array substrate device having a color filter on a thin film transistor (COT) structure for use in a liquid crystal display device, comprising:

a substrate having a display area, a non-display area, and a boundary area, the boundary area disposed between the display area and the non-display area;

a plurality of gate lines on the substrate in the display area;

a plurality of gate pads on the substrate in the non-display area;

a plurality of gate link lines on the substrate disposed in the non-display area and in the boundary area, each of the gate link lines connects one of the gate lines to one of the gate pads;

a plurality of data lines crossing the gate line and defining a plurality of pixel regions;

a plurality of thin film transistors near the crossings of the gate and data lines and including a gate electrode, an active layer, a source electrode, and a drain electrode;

a black matrix above the thin film transistors, the gate lines, and the data lines;

a plurality of color filters disposed in the pixel regions;

a light-shielding pattern disposed in the non-display area and the boundary area corresponding to spaces between the gate link lines;

an inorganic insulator on the black matrix and the light-shielding pattern; and

a plurality of pixel electrodes disposed in the pixel regions, each of the pixel electrodes contacting the drain electrode of the thin film transistor.

34. The device according to claim 33, further comprising an interlayer insulator between the black matrix and the thin film transistors and including an inorganic material selected from a group consisting of silicon nitride and silicon oxide.

35. The device according to claim 33, wherein the light-shielding pattern completely covers the spaces between the gate link lines to prevent light leakage.

36. The device according to claim 33, further comprising a seal pattern on the inorganic insulator, wherein the inorganic insulator includes a material selected from a group consisting of silicon nitride and silicon oxide.

37. The device according to claim 36, wherein the seal pattern directly contacts the gate link lines.

38. The device according to claim 33, wherein the pixel electrode includes a double-layered transparent conductive material having first and second layers, and each of the color filters are disposed between the first and second layers.